What is claimed is:

1. An MPEG video decoding system comprising:

a buffer for storing an MPEG-formatted video signal or a DV-formatted video signal;

a VLD/IQ means for performing a variable length decoding and an inverse quantization to the video signal outputted from the buffer;

an IDCT means for selectively performing an 8×8 IDCT and a 4×8 IDCT according to the format of the inversely quantized signal;

an adder for bypassing and storing the output signal of the IDCT means into an external memory if the output signal of the IDCT means is an MPEG-formatted I-picture or a DV format, and for adding the IDCT-ed signal and a motion compensated signal and storing the added signal into the external memory if the output signal of the IDCT means is an MPEG-formatted P-picture or an MPEG-formatted B-picture; and

a motion compensator for performing a motion compensation by using a motion information and a previous frame stored in the external memory and outputting the motion compensated signal to the adder if the output signal of the IDCT means is the MPEG-formatted P-picture or the MPEG-formatted B-picture.

2. The MPEG video decoding system of claim 1, wherein the IDCT means includes:

a horizontal 8×1 IDCT unit for performing an 8×1 IDCT to the inversely quantized video signal in a horizontal direction;

a transverse buffer for performing a horizontal-vertical transposition to the horizontally IDCT-ed signal;

a switching unit for controlling an output path of the signal outputted from the transverse buffer according to the format type of the inputted signal;

a vertical 8×1 IDCT unit for performing an 8×1 IDCT to the output signal of the switching unit in a vertical direction; and

a vertical 4×1 IDCT unit for performing a 4×1 IDCT to the output signal of the switching unit in a vertical direction.

3. The MPEG video decoding system of claim 2, wherein the format type of the inputted signal is one of an MPEG format, a vertical frame DCT of 625-50 DV format, a vertical frame DCT of 525-60 DV format, and a vertical field DCT of 525-60 DV format.

4. The MPEG video decoding system of claim 3, wherein if the format type of the inputted signal is the MPEG format, the vertical frame DCT of 625-50 DV format and the vertical frame DCT of 525-60 DV format, the switching unit outputs an output signal of the transverse buffer to the 8×1 IDCT unit, and if the format

type of the inputted signal is the vertical field DCT of 525-60 DV format, the switching unit outputs the output signal of the transverse buffer to the 4×1 IDCT.

5. The MPEG video decoding system of claim 1, further comprising a format converter, wherein the format converter converts a video-decoded 4:2:0 color difference signal into a 4:2:2 color difference signal if the video-decoded signal is the MPEG format or a 625-50 DV format, and converts a video-decoded 4:1:1 color difference signal into a 4:2:2 color difference signal if the video-decoded signal is a 525-60 DV format.

6. The MPEG video decoding system of claim 1, further comprising a de-shuffler, wherein if the video-decoded signal is a 525-60 DV format, the de-shuffler outputs the video-decoded signal by supper block unit consisting of a plurality of macro blocks, performs a de-shuffling to the video-decoded signal in order to reconfigure an original screen, and stores the de-shuffled signal into the external memory.

7. An MPEG video decoding system including a memory interface for controlling data input/output between a video decoder and an external memory, the MPEG video decoding system comprising:

an MPEG system decoder for dividing an external input MPEG bitstream into a video bitstream and an audio bitstream;

a DV system decoder for converting an external input DV formatted signal into a DIF signal and dividing the DIF signal into a video DIF and an audio DIF;

a single combined DV/MPEG video decoder for sharing a plurality of internal blocks to decode both the MPEG video signal outputted from the MPEG system decoder and the video DIF signal outputted from the DV system decoder and storing the decoded data into the external memory; and

a format converter for performing a format conversion to a color difference signal, the color difference signal being a signal that is video-decoded by the combined DV/MPEG video decoder and outputted through the external memory.

8. The MPEG video decoding system of claim 7, wherein the MPEG bitstream is inputted to the MPEG system decoder through a tuner, and the DV formatted signal is inputted to the DV system decoder through an IEEE-1394 interface.

9. The MPEG video decoding system of claim 7, wherein the combined DV/MPEG video decoder includes:

a buffer for temporarily storing a video signal outputted from one of the MPEG system decoder and the DV system decoder;

a VLD/IQ means for performing a variable length decoding and an inverse quantization to the video signal outputted from the buffer;

an IDCT means for performing an 8×8 IDCT if the inversely quantized signal is an MPEG format or 625-50 DV format, and performing one of an 8×8 IDCT and an 4×8 IDCT according to a DCT type if the inversely quantized signal is a 525-60 DV format;

an adder for bypassing and storing the output signal of the IDCT means into an external memory if the output signal of the IDCT means is an MPEG-formatted I-picture or a DV format, and adding the IDCT-ed signal and a motion compensated signal and storing the added signal into the external memory if the output signal of the IDCT means is an MPEG-formatted P-picture or an MPEG-formatted B-picture; and

a motion compensator for performing a motion compensation by using a motion information and a previous frame stored in the external memory and outputting the motion compensated signal to the adder if the output signal of the IDCT means is the MPEG-formatted P-picture or the MPEG-formatted B-picture.

10. The MPEG video decoding system of claim 9, wherein the IDCT means includes:

a horizontal 8×1 IDCT unit for performing an 8×1 IDCT to the inversely quantized video signal in a horizontal direction;

a transverse buffer for performing a horizontal-vertical transposition to the horizontally IDCT-ed signal;

a switching unit for controlling an output path of the signal outputted from the transverse buffer according to the format type of an inputted signal;

a vertical 8×1 IDCT unit for performing an 8×1 IDCT to the output signal of the switching unit in a vertical direction; and

a vertical 4×1 IDCT unit for performing a 4×1 IDCT to the output signal of the switching unit in a vertical direction.

11. The MPEG video decoding system of claim 10, wherein if the format type of the inputted signal is the MPEG format, a vertical frame DCT of 625-50 DV format and the vertical frame DCT of 525-60 DV format, the switching unit outputs an output signal of the transverse buffer to the 8×1 IDCT unit, and if the format type of the inputted signal is a vertical field DCT of 525-60 DV format, the switching unit outputs the output signal of the transverse buffer to the 4×1 IDCT.

12. The MPEG video decoding system of claim 7, wherein the format converter converts a video-decoded 4:2:0 color difference signal into a 4:2:2 color difference signal if the video-decoded signal is the MPEG format or a 625-50 DV format, and converts a video-decoded 4:1:1 color difference signal into a 4:2:2 color

difference signal if the video-decoded signal is a 525-60 DV format.

13. The MPEG video decoding system of claim 7, wherein if the video-decoded signal is a 525-60 DV format, the de-shuffler outputs the video-decoded signal by supper block unit consisting of a plurality of macro blocks, performs a de-shuffling to the video-decoded signal in order to reconfigure an original screen, and stores the de-shuffled signal into the external memory.